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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,695	09/30/2003	Fu-Chieh Hsu	MST-013-1D	8152

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BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,695	HSU, FU-CHIEH	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) 1 and 2 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 3-5 and 7-11 is/are rejected.

7)☒ Claim(s) 6 and 12 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0903.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 3 is objected to because of the following informalities: Claim 3 recites the limitation "body regions" in next to last line. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3-5 and 7-9 are rejected under 35 USC § 102(b) as being anticipated by Subbanna, U.S. Patent No. 5,789,286.

With regards to claim 3, Subbanna illustrates in figures 1 and 2 (entire document) forming a buried region 13 having a first conductivity type N below an upper surface of a semiconductor region 11 of a semiconductor substrate 10, the semiconductor region having a second conductivity type P, opposite the first conductivity type; and forming a field-effect transistor 16 in the semiconductor region over the buried region, wherein a depletion region MD is located between the buried region and source 21, drain 22 and body regions 23 of the field-effect transistor.

With regards to claims 4 and 5, Subbanna discloses in col. 4, lines 34-42, the buried region 13 is formed by an ion implantation step, wherein the buried region is implanted through a first mask.

With regards to claim 7, Subbanna illustrates in figs. 1 and 2 forming one or more shallow trench isolation regions 12 that extend a first depth d into the semiconductor substrate.

With regards to claim 8, Subbanna illustrates in fig. 2 implanting the buried region 13 such that the buried region has a top interface "j" located at or above the first depth in the semiconductor substrate, and a bottom interface located below the first depth in the semiconductor substrate.

With regards to claim 9, Subbanna discloses in col. 4, lines 31-33, the field-effect transistor 16 is fabricated using a process compatible with a standard CMOS process.

Claims 3, 10 and 11 are rejected under 35 USC § 102(b) as being anticipated by Kenney, U.S. Patent No. 5,264,716.

With regards to claim 3, Kenney illustrates in figures 1-12, particularly figure 1, (entire document) forming a buried region 32 having a first conductivity type N below an upper surface of a semiconductor region 12 of a semiconductor substrate 10, the semiconductor region having a second conductivity type P, opposite the first conductivity type; and forming a field-effect transistor 14 in the semiconductor region over the buried region, wherein a depletion region is located between the buried region and source 18, drain 20 and body regions 16 of the field-effect transistor.

With regards to claim 10, Kenney illustrates in fig. 1 forming a well region 24 having the first conductivity type N in the semiconductor substrate 10, wherein the buried region 32 contacts the well region.

With regards to claim 11, Kenney illustrates in fig. 1 forming a deep well region 24 having the first conductivity type N in the semiconductor substrate 10, wherein the deep well region is located below and continuous with the buried region 32.

Allowable Subject Matter

Claims 6 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hsu et al. (illustrates SRAM with a buried layer).

Field of Search	Date
U.S. Class and subclass: 438/238, 239, 386	October 25, 2004
Other Documentation: None	N/A
Electronic data base(s): EAST (USPAT, US-PGPUB, JPO, EPO, Derwent, IBM TDB)	October 25, 2004

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
October 25, 2004